

CLOCK GENERATOR

Om P. Agrawal

Hans W. Klein

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Technical Field

The present invention relates generally to electrical circuits and, more particularly, to clock generators.

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Background

Clock generator circuits are typically employed to generate one or more clock output signals based upon a clock input signal. One drawback of conventional clock generator circuits (e.g., clock generator integrated circuits or chips) is their limited programmability.

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For example, there is often limited programmability in terms of input/output signal types, input/output voltage levels, frequency range, and/or output banking structure. Furthermore, if programming is available, the programming may have to be performed by pin strapping, which is difficult to implement, inflexible, and may require the utilization of a number of pins.

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Another drawback of conventional clock generator circuits is their lack of support for joint test action group (JTAG) or other automated testing. Consequently, it can often be cumbersome, time-consuming, and expensive to test a circuit board having clock generator circuits and other components (e.g., microprocessors, field programmable gate arrays (FPGAs), or complex programmable logic devices (CPLDs)). As a result, there is a need for improved clock generation techniques.

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SUMMARY

Systems and methods are disclosed herein to provide clock generation. For example, in accordance with an embodiment of the present invention, a clock generator chip is provided that is configurable and in-system programmable to provide programmable input circuits, programmable output circuits, and permit a JTAG boundary scan. The clock generator chip may be configurable by employing on-chip electrically erasable memory (e.g., electrically erasable programmable read only memory (EEPROM)). The programmable input circuits permit a wide variety of input voltage levels, input signal types, and input frequency range. The programmable output circuits permit a wide variety of output voltage levels, output signal types, and output frequency. The clock generator chip may also have flexible output banking structures and a programmable output impedance.

More specifically, in accordance with one embodiment of the present invention, a clock generator includes a first circuit adapted to receive an input signal, having a possible range of voltage levels and signal types, and modify a frequency of the input signal by a first programmable amount to generate a first input signal; a feedback loop circuit adapted to receive a feedback signal and modify a frequency of the feedback signal by a second programmable amount to generate a second input signal; a phase-locked loop circuit adapted to receive the first input signal and the second input signal and provide a first output signal; and a second circuit adapted to receive the first output signal and modify a frequency of the first output signal to generate a plurality of second output signals having programmable frequencies, wherein the first and second

programmable amount and the programmable frequencies are determined by data stored in electrically erasable memory.

In accordance with another embodiment of the present invention, an integrated circuit includes means for selecting
5 from a plurality of input signals and generating a first input signal having a programmable frequency; means for selecting from a plurality of feedback signals and generating a second input signal having a programmable frequency; a phase-locked loop adapted to receive the first input signal and the second input
10 signal and generate a first output signal; means for receiving the first output signal and generating second output signals having programmable frequencies; means for selecting from the second output signals and providing output signals each having a programmable voltage level, signal type, and output impedance;
15 and means for providing configurability and in-system programmability.

In accordance with another embodiment of the present invention, a method of generating clock signals includes receiving an input signal, wherein the input signal may be a
20 single-ended signal type or a differential signal type; modifying a frequency of the input signal by an amount determined from data selected from memory to provide a first input signal; receiving a feedback signal; modifying a frequency of the feedback signal by an amount determined from data
25 selected from memory to provide a second input signal; aligning a frequency and/or a phase of the first input signal and the second input signal to provide a first output signal; modifying a frequency of the first output signal to generate a plurality of second output signals having frequencies determined from data
30 selected from memory; and providing output signals, selected from the second output signals, which have programmable voltage levels, signal types, and output impedances.

In accordance with another embodiment of the present invention, a clock generator includes an input circuit programmable to receive input signals of various signal types and voltage levels and to generate in response an input signal
5 to a phase-locked loop (PLL); a phase-locked loop adapted to receive the PLL input signal and to generate in response a PLL output signal; and an output circuit adapted to receive the PLL output signal and be programmable to generate in response clock signals of various signal types and voltage levels.

10 The scope of the invention is defined by the claims, which are incorporated into this section by reference. A more complete understanding of embodiments of the present invention will be afforded to those skilled in the art, as well as a realization of additional advantages thereof, by a consideration
15 of the following detailed description of one or more embodiments. Reference will be made to the appended sheets of drawings that will first be described briefly.

BRIEF DESCRIPTION OF THE DRAWINGS

20 Fig. 1 shows a block diagram illustrating a clock generator circuit in accordance with an embodiment of the present invention.

Fig. 2 shows a block diagram illustrating a more detailed exemplary implementation of the clock generator circuit of Fig.
25 1 in accordance with an embodiment of the present invention.

Fig. 3 shows a block diagram illustrating frequency selection for a clock generator circuit in accordance with an embodiment of the present invention.

Fig. 4 shows a block diagram illustrating frequency selections for a clock generator circuit in accordance with an embodiment of the present invention.

5 Fig. 5 shows a block diagram illustrating an exemplary output circuit for a clock generator circuit in accordance with an embodiment of the present invention.

Fig. 6 shows a block diagram illustrating an exemplary output circuit for a clock generator circuit in accordance with an embodiment of the present invention.

10 Fig. 7 shows a block diagram illustrating an exemplary output circuit with output impedance control for a clock generator circuit in accordance with an embodiment of the present invention.

15 Fig. 8 shows a block diagram illustrating an exemplary input circuit for a clock generator circuit in accordance with an embodiment of the present invention.

Fig. 9 shows a block diagram illustrating an exemplary input circuit for a clock generator circuit in accordance with an embodiment of the present invention.

20 Fig. 10 shows a block diagram illustrating an exemplary input circuit for a clock generator circuit in accordance with an embodiment of the present invention.

25 Fig. 11 shows a block diagram illustrating an exemplary input boundary scan cell circuit for a clock generator circuit in accordance with an embodiment of the present invention.

Fig. 12 shows a block diagram illustrating an exemplary input boundary scan cell circuit for a clock generator circuit in accordance with an embodiment of the present invention.

Fig. 13 shows a block diagram illustrating an exemplary input boundary scan cell circuit for a clock generator circuit in accordance with an embodiment of the present invention.

5 Fig. 14 shows a block diagram illustrating an exemplary input boundary scan cell circuit for a clock generator circuit in accordance with an embodiment of the present invention.

Fig. 15 shows a block diagram illustrating an exemplary output boundary scan cell circuit for a clock generator circuit in accordance with an embodiment of the present invention.

10 The preferred embodiments of the present invention and their advantages are best understood by referring to the detailed description that follows. It should be appreciated that like reference numerals are used to identify like elements illustrated in one or more of the figures.

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DETAILED DESCRIPTION

Fig. 1 shows a block diagram illustrating a clock generator circuit 100 in accordance with an embodiment of the present invention. Clock generator circuit 100 may be formed as a
20 separate integrated circuit (chip) or formed as part of a larger integrated circuit to provide clock signals (internally or externally), while the larger chip also performs its other intended functions.

Clock generator circuit 100 includes an input clock divider
25 (M) 102, a feedback loop divider (N) 104, a phase-locked loop (PLL) core 106, dividers 108, and in-system programmable (ISP) and JTAG circuits 110. Clock generator circuit 100 receives reference signals and external feedback signals via leads 112, control signals via leads 114, and JTAG or ISP input signals via

leads 116. Clock generator circuit 100 provides output signals via leads 120 and JTAG and other signals via leads 118.

In general, clock divider 102 modifies a frequency of an input signal, such as a reference clock signal, by a programmable and selectable amount and provides the input signal to PLL core 106, while feedback loop divider 104 divides an external or internal feedback signal by a programmable and selectable amount and provides the feedback signal to PLL core 106. PLL core 106 provides frequency and/or phase lock based on the signals provided by clock divider 102 and feedback loop divider 104 and generates an output signal, which is divided by a programmable amount by dividers 108 to provide selectable output signals via leads 120. It should be understood that clock divider 102, feedback loop divider 104, and divider 108 may be designed to multiply, divide, and/or leave unchanged a frequency of an input signal depending upon the desired application.

Clock generator circuit 100 is in-system programmable and configurable (e.g., by electrically erasable memory) to provide a flexible clock generation system. For example, input signals received by leads 112 and 114 may be of various signal types (e.g., LVCMOS, LVTTL, SSTL, HSTL, LVDS, and LVPECL) and voltage levels (e.g., 1.8V, 2.5V, and 3.3V). PLL core 106 along with clock divider 102, feedback loop divider 104, and dividers 108 are also programmable and configurable to provide various selectable clock frequencies. Output signals may also be of various signal types and voltage levels, as discussed similarly above for the input signals, and also provide a programmable impedance control. Circuits 110 provide the ISP functionality and test functionality for clock generator circuit 100.

Fig. 2 shows a block diagram illustrating a clock generator circuit 200, which is a more detailed exemplary implementation

for portions of clock generator circuit 100 of Fig. 1. Clock generator circuit 200 selects a desired reference input signal (REFIN) via input circuits 218 and a multiplexer 210 to provide to a clock divider 202, which programmably divides its frequency and provides the reference input signal to a PLL core 206 and to a multiplexer 216. Multiplexer 216 selects between clock divider 202 (e.g., during system test or debug purposes) and PLL core 206 to route their corresponding output signal to a divider 208.

10 A multiplexer 212 selects a desired feedback signal (FBIN), which is provided to a multiplexer 214 that selects between the feedback signal (via input circuits 220) and an internal feedback signal and provides a selected signal to a feedback loop divider 204. Feedback loop divider 204 programmably
15 divides a frequency of the selected signal and provides it to PLL core 206.

PLL core 206 includes a phase frequency detector (PFD), a current charge pump and loop filter (ICP), and a voltage controlled oscillator (VCO). PLL core 206 may also have a
20 programmable output frequency range by utilizing an internal voltage divider. A lock signal is provided when PLL core 206 achieves frequency and phase lock.

Divider 208 divides a signal received from multiplexer 216 and provides clock signals having different frequencies that are
25 selectable by multiplexers 222 and driven out by output circuits 226. Skew control for the output signals may be provided by skew circuits 224 and skew circuit 228.

An output enable signal 232 is provided for each output circuit 226. For example, if output enable signal 232 is
30 asserted, then the output signals from output circuit 226 are synchronously enabled. If output enable signal 232 is

deasserted, then the output signals from output circuit 226 are synchronously disabled.

In general, clock generator circuit 200 provides programmable features, such as programmable frequency range, programmable input/output signal types and voltage levels, and programmable output impedance. PLL core 206 may be a fully integrated, high performance PLL core that can be configured as a zero delay buffer, a multiplier or a divider, and have programmable output frequencies. For example, clock generator circuit 200 may provide 20-buffered output signals from one master clock, with each buffered output signal driving a terminated transmission line.

Clock divider 202, feedback loop divider 204, and divider 208 are each programmable to allow very flexible output-to-input frequency ratios (e.g., 1 to 32). Furthermore, an external feedback path allows clock generator circuit 200 to achieve a zero delay between the reference input and the selected feedback output clock signal.

In this example (Fig. 2), output circuits 226 are arranged in ten banks, each with two possible output signal paths (e.g., one differential signal or two single-ended signals per bank). As shown, an additional bank is included to provide an internal feedback path for feedback loop divider 204. Each bank may have its own separate supply voltage (Vcco) and ground (Gndo) pins so that the output signals of the bank may support various output voltage levels (e.g., 1.8V, 2.5V, and 3.3V) independently of the other banks. Thus, for this example (ten banks, two output signal paths per bank), there are twenty possible output signals (if the banks are all configured as single-ended), which require ten separate supply voltages and grounds.

Input circuits 218 and 220 and output circuits 226 may be configured independently to support single-ended or differential standards (e.g., LVTTL, LVCMOS, HSTL, SSTL, LVPECL, and LVDS), which permits single-ended input to single-ended output, single-ended input to differential output, differential input to single-ended output, and differential input to differential output. Output circuits 226 may also have a programmable output impedance (e.g., to accommodate transmission-line impedance from 40 to 70 ohms in 5 ohm increments). Thus, output circuits 226 may be able to drive transmission lines of 50 ohm impedance without requiring external on-board series resistors, which reduces parts and implementation costs along with implementation time and effort. Output circuits 226 may also provide an independent clock invert function.

A profile select signal 230, as shown in Fig. 2, is provided to, for example, control multiplexers 222 and also clock divider 202 and feedback loop divider 204. Profile select signal 230 controls multiplexers 222 to perform frequency selection by, for example, selecting from up to four different sets of frequencies from divider 208. Likewise, profile select signal 230 may also control clock divider 202 and feedback loop divider 204 by selecting from one set of four registers to provide control signals for each. In addition, profile select signal 230 may also control the skew settings by selecting one set of four registers that define the various skew parameters.

For example, Fig. 3 shows a block diagram illustrating frequency selection for clock generator circuit 200 in accordance with an embodiment of the present invention. Profile select signal 230 is routed to multiplexers 302, 306, and 310 corresponding to clock divider 202, feedback loop divider 204, and divider 208, respectively. A number of registers 304, 308, and 312 are associated with clock divider 202, feedback loop

divider 204, and divider 208, respectively, to select a desired division ratio.

As an example, clock divider 202 and feedback loop divider 204 may each have division ratios from 1 to 32 and divider 208 may have division ratios from 2, 4, 6, ..., to 64. Profile select signal 203 (e.g., a 2-bit signal) controls multiplexer 302 to select signals from one of four 5-bit registers 304, which determines the division ratio for clock divider 202. Similarly, profile select signal 203 controls multiplexers 306 and 310 to select signals from one of four 5-bit registers 308 and 312, which determine the division ratio for feedback loop divider 204 and divider 208, respectively. For example, registers 308 may store four 5-bit values, selected from the range of 00000 to 11111, which correspond to division ratios from 1 to 32, respectively.

Registers 304, 308, and 312 are each configurable to store 4 of 32 possible settings for clock divider 202, feedback loop divider 204, and divider 208. Thus, a user may configure registers 304, 308, and 312 with appropriate settings to produce desired clock frequencies, which are selectable via profile select signal 203. These settings stored by registers 304, 308, and 312 may be changed by in-system programming techniques whenever a user desires. Registers 304, 308, and 312 may, for example, be electrically erasable registers (e.g., formed by EEPROM).

These techniques may be applied a number of times, depending upon the number of selectable output clock frequencies desired. For example, if five different output clock frequencies are desired, divider 208, multiplexer 310, and registers 312 may be repeated four more times (as shown in Fig. 4) to provide the five possibly different output clock frequencies (freq-0 through freq-4). Thus, profile select

signal 230 (labeled FS pins) may function as a select signal for multiplexer 310 for tapping 1 of 32 different tap points (frequency output points) of divider 208 to select each frequency.

5 By having a number of banks and a number of frequencies to select from, a flexible banking output structure may be provided. For example, if ten banks and five frequencies are available, a user can select how to group the banks and the number of output signals of various frequencies based upon a
10 particular application. As an example, the ten banks may be configured to operate as one bank (e.g., same output voltage levels, signal types, and output impedance) at one frequency to provide 20 output signals. As another example, the ten banks may be configured to operate as two banks at one frequency or at
15 two different frequencies to provide 10 output signals from each bank. Thus, various combinations of banking output structure, voltage levels, signal types, frequencies, output impedance, etc. may be selected based upon techniques discussed herein in accordance with one or more embodiments of the present
20 invention.

For this particular implementation having ten banks, there could be up to ten or twenty different frequencies depending upon whether the banks are configured as differential or single-ended, respectively. However, the number of different
25 frequencies available for the banks may be limited. As shown in Fig. 2, profile select signal 230 controls multiplexers 222 to select from among the possible output clock frequencies generated by divider 208. Consequently, the number of different frequencies available simultaneously is limited by the number of
30 dividers 208 (or number of different frequencies provided by divider 208).

As discussed above for one exemplary implementation, the frequency range of operation for clock generator circuit 200 is determined by profile select signal 230 and configuration bits stored by registers 304, 308, and 312. Thus, four different
5 profiles may be selected for each bank by profile select signal 230.

It should be understood that numerous modifications and variations are possible with respect to one or more of the embodiments discussed in reference to Fig. 2. For example,
10 rather than be limited by profile select signal 230 having only two bits, one or more control signals may be implemented to allow the independent selection of the entire range of division or multiplication ratios for clock divider 202, feedback loop divider 204, and divider 208, and also allow the selection from
15 all of the possible frequencies from divider 208 for any of output circuits 226. However, this would require a number of additional control signal paths (e.g., external leads) along with possibly additional circuitry, board space, and implementation complexity. Thus, one or more of these
20 disadvantages may be avoided and a user may be able to obtain desired clock signals by utilizing one or more of the techniques discussed herein (e.g., as shown in Figs. 3 and 4), including configurability and in-system programmability.

As shown in Fig. 2, input circuits 218 and 220 and output
25 circuits 226 are provided to programmably support a wide range of signal types and signal levels. For example, the signal types may include un-terminated single-ended interfaces (e.g., LVTTTL and LVCMOS), terminated single-ended interfaces (e.g., SSTL and HSTL, which require a voltage reference signal and
30 possibly a termination voltage signal), and differential interface standards (e.g., LVDS and LVPECL). The signal types

may also include DDR and QDR memory interface signals, such as differential HSTL or SSTL (e.g., to drive SDRAMs and SRAMs).

For example, Figs. 5-7 show exemplary implementations for one of output circuits 226 (i.e., for one bank) for clock generator circuit 200 of Fig. 2 in accordance with an embodiment of the present invention. Fig. 5 illustrates an exemplary implementation employing a differential output buffer in conjunction with a pair of single-ended output buffers, which may be utilized to support various signal types. Fig. 6 shows a modification to the implementation of Fig. 5 to support differential HSTL, SSTL, and LVDS with the same output buffer.

Fig. 7 shows a modification to the implementation of Figs. 5 and 6 by including two separate differential output buffers (rather than the one differential output buffer of Figs. 5 and 6). A variable resistance (labeled RS in Figs. 5-7) represents a programmable output impedance of the single-ended output buffer, which may be matched to a line impedance for series termination. The output impedance, for example, may have an impedance range from 40 to 70 ohms in 5 ohm steps.

Referring to Fig. 2, input circuits 218 and 220 may receive (for this exemplary application) four pairs of differential or four single-ended input signals. For example, when configured to receive a single-ended input signal, input circuit 218 or input circuit 220 receives a signal on one input terminal, while the other input terminal is unused or receives a reference voltage, depending upon the application or programmed input specification. Fig. 8 shows a block diagram illustrating an input circuit 800, which is an exemplary implementation for one of four input circuits 218 or 220 shown in Fig. 2 in accordance with an embodiment of the present invention. A VCM/VTT pin is provided, with VCM (common mode voltage) for differential signals and with VTT (termination voltage) for certain types of

single-ended signals (e.g., HSTL). A resistance (RT) is programmable, with for example a nominal center point of 50 ohm. As an example, Figs. 9 and 10 illustrate exemplary applications for input circuit 800.

5 Clock generator circuit 100 (Fig. 1) and clock generator circuit 200 (Fig. 2), in accordance with an embodiment of the present invention, may be implemented to be compliant with JTAG testing, such as IEEE 1149.1 standards (e.g., IEEE 1149.1-1993 standard). Additionally, clock generator circuits 100 and 200
10 may also be compliant with IEEE 1532 standard describing configuration of programmable logic devices.

For JTAG support, Fig. 11 shows a block diagram illustrating an exemplary input boundary scan cell circuit 1100 for a clock generator circuit in accordance with an embodiment
15 of the present invention. Circuit 1100 allows instructions to be performed, for example, as outlined in the JTAG standard (IEEE 1149.1-1993, e.g., sample/preload and EXTEST). Specifically, circuit 1100 in Fig. 11 illustrates exemplary circuit operation during an EXTEST function (capture-DR).

20 Fig. 12 illustrates exemplary circuit operation for circuit 1100 during sample/preload (for capture-DR (CDR), shift-DR (SDR), and update-DR (UDR)). Similarly, Figs. 13 and 14 illustrate exemplary circuit operation for circuit 1100 during EXTEST (for CDR, SDR, and UDR) and INTEST (for CDR, SDR, and
25 UDR), respectively. Note that in Figs. 11-14, shift/test paths are indicated by "S/T" and data flow is indicated by "D" while shaded multiplexers are considered do not care for that particular situation.

Fig. 15 shows a block diagram illustrating an exemplary
30 output boundary scan cell circuit 1500 for a clock generator circuit in accordance with an embodiment of the present

invention. Circuit 1500, for example, supports full EXTEST and modes of operation, but does not support INTEST as the pins are output only.

5 In general, boundary scan cells (e.g., circuit 1100 and/or circuit 1500) are inserted appropriately on all input/output paths, clock paths, and dedicated input paths, except for voltage supply leads and four dedicated 1149.1 TAP pins. The boundary scan cells provide IEEE 1149.1 compliance and allow functional testing of the circuit board, on which the device
10 (e.g., clock generator circuit 100) is mounted, through a serial scan path that can access all critical logic nodes. Internal registers may be linked internally, which allows test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. The
15 device may also be linked into a board-level serial scan path for more board-level testing.

As noted above, the device may also provide in-system programming (ISP) capability (e.g., IEEE 1532 compliant ISP). For example, the ISP capability may be provided through the
20 boundary scan test access port. The ISP capability provides a number of significant benefits, such as for example rapid prototyping, lower inventory levels, higher quality, and the ability to make in-field modifications.

In accordance with one or more embodiments of the present
25 invention, a configurable (e.g., via EEPROMs) and in-system programmable clock generator (e.g., circuit or chip) is provided. The clock generator may provide flexible programmable inputs that permit various input voltage levels, input signal types, and input frequency range. The clock generator may
30 provide flexible programmable outputs that permit various output voltage levels, output signal types, and output frequency range. Furthermore, flexible output banking structures may be provided

along with a programmable output impedance. The clock generator may also permit JTAG or other automated testing.

Embodiments described above illustrate but do not limit the invention. It should also be understood that numerous

5 modifications and variations are possible in accordance with the principles of the present invention. Accordingly, the scope of the invention is defined only by the following claims.